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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/528,285	03/16/2005	Stephen J. Battersby	14509-0127US1 / P080482SE	6607

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EXAMINER	
CHOW, YUK	

ART UNIT	PAPER NUMBER
2629	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATDOCTC@fr.com

Office Action Summary	Application No.	Applicant(s)	
	10/528,285	BATTERSBY ET AL.	
	Examiner	Art Unit	
	YUK CHOW	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 November 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,13-18 and 21-25* is/are rejected.

7)☒ Claim(s) *10-12,19 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 4-9 and 13-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Koyama et al. (US Patent 6,597,349).

As to **claim 1**, Koyama discloses an active matrix display, comprising:

an array of pixels provided over a common substrate (see Fig. 10A), each pixel comprising a display element and a switching device (Fig. 10(1002); and

a column driver (Fig. 10(1003)) for providing signals to the pixels for driving the display elements, the column driver comprising digital to analogue converter circuitry (see Fig. 2(208)) and providing a first number of display element drive levels greater than 2,

wherein each pixel comprises means for converting the first number of display element drive levels (Fig. 15(1507) into a second, greater number, of pixel grey levels (see Col. 21 lines 23-35).

As to **claim 4**, Koyama discloses a display as claimed in claim 1, wherein the means for converting comprises, within each pixel, charge redistribution circuit elements (See Fig. 2(207)).

As to **claim 5**, Koyama discloses a display as claimed in claim 4, wherein the charge redistribution elements comprise two display elements (Fig. 2(S0, S1)), an input switch (Fig. 2(209)) between the input to the pixel and a first display element and a charge redistribution switch (Fig. 2(210)) between the first and second display elements (see Col. 7 lines 37-55).

As to **claim 6**, Koyama discloses a display as claimed in claim 1, wherein the digital to analogue circuitry receives a 5 bit input (see Col. 23 lines 54-67, multi-bit DAC).

As to **claim 7**, Koyama discloses a display as claimed in claim 6, wherein the output of the digital to analogue circuitry comprises a number of levels less than 32 (It's inherent that 5-bit input could have 32 possible levels).

As to **claim 8**, Koyama discloses a display as claimed in claim 7, wherein the output digital to analogue circuitry comprises 22 possible levels (It's possible that 5-bit input could have 22 levels).

As to **claim 9**, Koyama discloses a display as claimed in claim 1 further comprising a converter for deriving from a 6 bit drive signal a signal for selecting which one or ones of the first number of levels to apply to each display element (see Col. 3 lines 3-15).

As to **claim 13**, Koyama discloses a display as claimed in claim 1, comprising a plurality of row conductors (Fig. 2(213)), a number of row conductors being associated with each row of pixels corresponding to the number of display elements within each pixel (see Fig. 2(214)).

As to **claim 14**, Koyama discloses a display as claimed in claim 1, wherein each pixel comprises a memory element (Fig. 2(203)) for storing digital drive values for the display elements of each pixel (see Col. 2 lines 61-67).

As to **claim 15**, Koyama discloses a display as claimed in claim 1, wherein the digital to analogue circuitry is provided on the common substrate (see Fig. 10A).

As to **claim 16**, Koyama discloses a display as claimed in claim 15, wherein the pixel array and the digital to analogue circuitry are formed using low temperature polysilicon processing (See Col. 17 line 65- Col. 18 line 3).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2-3, 17-18, 21-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koyama et al. (US Patent 6,597,349) in view of Silverbrook et al. (US Patent 5,805,136).

As to **claim 2**, Koyama discloses a display as claimed in claim 1 above.

However Kayama does not teach wherein the means for converting comprises, within each pixel, at least first and second display elements having different areas.

Silverbrook discloses an intermingling sub-pixels in discrete level display wherein teaches display elements having different area (See Fig. 17).

It would have been obvious to one ordinary skill in the art at the time of invention was made to incorporate display elements having different areas as in Silverbrook into semiconductor display device of Koyama, because a pixel layout design for a discrete level display providing a interfused arrangement of more intense members (see Col. 2 lines 6-19).

As to **claim 3**, Koyama and Silverbrook disclose a display as claimed in claim 2, wherein the first and second display elements have areas in the ratio 1:2 (see Fig. 17, level 7, having area ratio of 1:2).

As to **claim 17**, Koyama discloses a method of driving an active matrix display, comprising:

providing first and second drive voltages, the first and second drive voltages being selected from two adjacent drive voltage levels of a digital to analogue converter (Fig. 2(208)) which has more than 2 output levels (Fig. 2(210).

However Koyama does not teach a display pixel having first and second display elements, within the pixel generating an intermediate grey level corresponding to a drive voltage between the first and second levels.

Silverbrook discloses an intermingling sub-pixels in discrete level display wherein teaches a display pixel having multiple display elements (Fig. 9(36-45)) and intermediate grey level (See Fig. 17, level 2-level 14).

It would have been obvious to one ordinary skill in the art at the time of invention was made to incorporate multiple display element for generating intermediate grey level as in Silverbrook into semiconductor display device of Koyama, because a pixel layout

design for a discrete level display providing a interfused arrangement of more intense members (see Col. 2 lines 6-19).

As to **claim 18**, Koyama and Silverbrook disclose a method as claimed in claim 17, wherein the first display element has a first area and the second display element has a second area different to the first area, area weighting being used to generate the intermediate grey level (see Silverbrook Fig. 17, there are 14 level of intermediate grey level).

As to **claim 21**, Koyama and Silverbrook disclose a method as claimed in any one of claim 18, wherein a plurality of sub-rows of pixels are addressed in turn, each sub-row comprising respective display elements for each pixel (see Koyama Fig. 3).

As to **claim 22**, Koyama and Silverbrook disclose a method as claimed in any one of claim 18, wherein a plurality of rows of pixels are addressed in turn, each row being addressed once to address both display elements and a second time to readdress the second display element (see Koyama fig. 5).

As to **claim 23**, Koyama and Silverbrook disclose a method as claimed in claim 17, wherein charge sharing between the display elements is used to generate the intermediate grey level (It's inherently to share charge between different display elements to have different level of grey scale).

As to **claim 24**, Koyama and Silverbrook disclose a method as claimed in claim 23, wherein the first and second drive voltages are provided by a digital to analogue converter which receives a 5 bit input (see Col. 23 lines 54-67, multi-bit DAC).

As to **claim 25**, Koyama and Silverbrook disclose a method as claimed in claim 24, wherein the drive voltages are provided from a column driver circuit integrated onto the active plate of the active matrix display (See Fig. 10A).

Allowable Subject Matter

5. Claims 10-12, 19-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter: cited references do not teach or mention applicant's claimed limitation, "divider for dividing by 3 and providing a divisor and remainder" in claim 10 and 19.

Response to Arguments

7. Applicant's arguments filed 11/25/2008 regarding claim 1 have been fully considered but they are not persuasive.

Regarding claim 1, Applicant argues that Koyama does not describe "each pixel comprises means for converting the first number of display element drive levels into a second, greater number, of pixel grey levels". However, examiner respectfully disagrees. As applicant points to Col. 21 lines 25-26: "element 1507 is a level shifter circuit that raises the voltage level of the digital video data", an ordinary skill in the art will reasonably interpret **"raising the voltage level"** as **"converting level into a higher number"**.

As to claim 17, Applicant's argument regarding Koyama does not teach a pixel having first and second display element have been considered but moot in view of new

ground of rejection.

Applicant's argument regarding Silverbrook disclosure does not teach "intermediate grey level". However, examiner respectfully disagrees. According to Silverbrook description of generating a "intermediate grey level", 4-bit binary weight (see Col. 5 lines 25-38) is corresponding to drive between first level (lowest 0000) and second level (highest 1111). Therefore, an ordinary skill in art will reasonably interpret "intermediate grey level" as any level between minimum grey level and maximum grey level.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to YUK CHOW whose telephone number is (571)270-1544. The examiner can normally be reached on 8-6 M-TH E.T..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on 571 272-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Y. C./
Examiner, Art Unit 2629

/Amare Mengistu/

Supervisory Patent Examiner, Art Unit 2629